WHAT IS CLAIMED IS:

1. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire on an insulating substrate;

sequentially depositing a gate insulating layer, an amorphous silicon layer, a doped amorphous silicon layer and a metal layer in a vacuum state;

patterning the metal layer to form a data line, a source electrode and a drain electrode;

etching the doped amorphous silicon layer by using the data line, the source electrode and the drain electrode as etch stopper;

depositing a photoresist layer;

patterning the photoresist layer to cover at least the peripheries of the source electrode and the drain elecrode;

patterning the amorphous silicon layer;

forming a passivation layer having a contact hole that exposes a portion of the drain electrode; and

forming a pixel electrode connected to the drain electrode through the contact hole.

2. The method of claim 1, wherein the sequential deposition of the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer is performed using an equipment in which a sputter equipment and a chemical vapor deposition equipment are integrally formed.

3. The method of claim 1, wherein the patterning of the amorphous silicon layer further comprises:

forming a photoresist pattern having an extra width of 0.1 to 0.4 μm after completely covering the source electrode and the drain electrode and having a boundary line that is identical to or narrower than that of the data line; and

overetching the amorphous silicon layer to make a groove having a depth of 0.1 to 0.4 μm under the data line.

4. The method of claim 1, wherein the gate wire is a single layer and made of one among the group of aluminum, an aluminum alloy, molybdenum, an molybdenum alloy, chromium, a chromium alloy, tantalum and a tantalum alloy, or double-layered and made of any two of the above described materials.

5. A method of manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire on an insulating substrate;

sequentially depositing a gate insulating layer, an amorphous silicon layer, a doped amorphous silicon layer and a metal layer in a vacuum state;

patterning the metal layer to form a data line, a source electrode and a drain electrode;

depositing a photoresist layer;

patterning the photoresist layer to cover at least the peripheries of the source electrode and the drain electrode;

simultaneously patterning the doped amorphous silicon layer and the amorphous silicon layer;

removing the photoresist layer pattern;

etching the doped amorphous silicon layer by using the data line, the

source electrode and the drain electrode as an etch stopper;

forming a passivation layer having a contact hole that exposes a portion of the drain electrode; and

forming a pixel electrode connected to the drain electrode through the contact hole.

6. The method of claim 5, wherein the sequential deposition of the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer is performed by using an equipment in which a sputter equipment and a chemical vapor deposition equipment are integrally formed.

7. The method of claim 5, wherein the patterning of the amorphous silicon layer further comprises:

forming a photoresist pattern having a width redundancy of 0.1 to 0.4 μm after completely covering the source electrode and the drain electrode and having a boundary line that is identical to or narrower than that of the data line; and

overetching the amorphous silicon layer to make a groove having a depth of 0.1 to 0.4 μm under the data line.

8. The method of claim 5, wherein the gate wire is a single layer and made of one among the group of aluminum, an aluminum alloy, molybdenum, an molybdenum alloy, chromium, an chromium alloy, tantalum and an tantalum alloy, or double-layered and made of any two of the above described materials.

9. An apparatus for depositing a layer on a substrate, comprising;

a loadlock chamber that receives a substrate;

a preheat chamber that heats the substrate before deposition;

a process chamber that deposits a layer on the substrate; and

a sputter chamber that deposits a metal layer on the substrate,

wherein the substrate is transferred among the chambers in a vacuum while not exposed to ambient atmosphere.